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10ES32

Third Semester B.E. Degree Examination, Dec.2017/Jan.2018
Analog Electronic Circuits

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Using Shockley's equation, determine the diode current at 25°C for a silicon diode with $I_S = 20$ pA and $V_D = 0.7$ V. Find the same when $V_D = 0.5$ V. **(04 Marks)**

b. Sketch the output waveform for the following circuit shown in Fig. Q1 (b), and plot the transfer characteristics - **(06 Marks)**

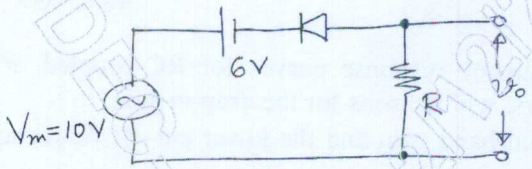

Fig. Q1 (b)

c. Check the condition for the following circuit shown in Fig. Q1 (c) to work as clamper. Sketch the output waveform. **(05 Marks)**

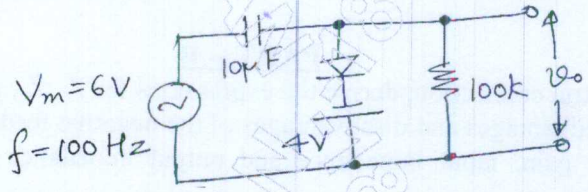

Fig. Q1 (c)

d. Find the current in the loop, the output voltage, and the power absorbed by each device. **(05 Marks)**

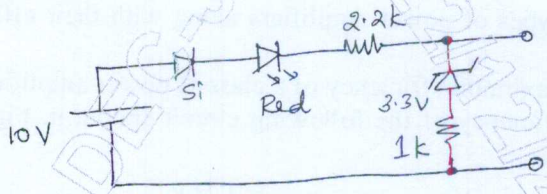

Fig. Q1 (d)

2 a. Derive the expression for I_B and V_{CE} of an emitter bias circuit. **(04 Marks)**

b. Check the condition for the approximate analysis of the voltage-divider bias circuit and obtain the Q-point using approximate analysis, given : $V_{CC} = +12$ V, $\beta = 120$, $R_C = 1.5\,K\Omega$, $R_E = 620\ \Omega$, $R_1 = 33$ kΩ and $R_2 = 4.7$ kΩ. Mark the Q-point on the DC load – line. **(06 Marks)**

c. Determine the values for the following circuit: V_E, I_E, V_{CE}, V_C, I_B and β. **(06 Marks)**

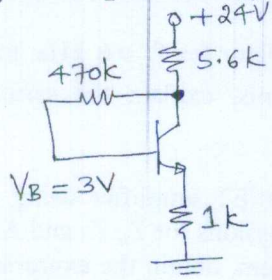

Fig. Q2 (c)

d. Design a fixed bias circuit for $V_{CC} = 10$ V, $\beta = 120$, $I_{C_Q} = 1.4$ mA and $V_{CE_Q} = 5$ V. **(04 Marks)**

3 a. Using r_e model, derive the expressions for Z_i, Z_o and A_V of a fixed bias circuit. **(06 Marks)**

b. Using exact analysis, determine Z_i, Z_o and A_V for the voltage-divider bias network if $R_1 = 220\ k\Omega$, $R_2 = 56\ k\Omega$, $R_C = 6.8\ k\Omega$, $R_E = 2.2\ k\Omega$, $\beta = 180$, $r_o = 50\ k\Omega$ and $V_{CC} = 20V$. **(10 Marks)**

c. For the network shown in Fig. Q3 (c), determine Z_i, Z_o and A_V. **(04 Marks)**

$h_{fe} = 150$
$h_{ie} = 2.75\ k\Omega$
$h_{Oe} = 25\ \mu S$

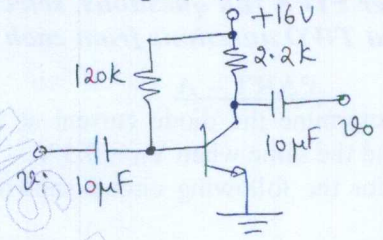

Fig. Q3 (c)

4 a. Explain the frequency response curves for RC-coupled, transformer-coupled and direct-coupled amplifiers, with reasons for the drop in gain. **(09 Marks)**

b. Determine the mid-band gain and the lower cut-off frequencies f_{L_S} and f_{L_C} for the voltage-divider bias BJT amplifier with $C_S = 10\ \mu F$, $C_C = 10\ \mu F$, $R_S = 1\ k\Omega$, $R_1 = 36\ k\Omega$, $R_2 = 8.2\ k\Omega$, $R_E = 1.5\ k\Omega$, $R_C = 4.7\ k\Omega$, $R_L = 2.2\ k\Omega$, $\beta = 100$ and $V_{CC} = 20V$. **(11 Marks)**

PART – B

5 a. For a Darlington connection, derive the expressions for Z_i, Z_o, A_i and A_V. **(12 Marks)**

b. Mention the advantages and disadvantages of the negative feedback. **(04 Marks)**

c. Calculate the gain, input impedance and output impedance of a voltage-series-feedback amplifier having A = -300, $R_i = 1.5\ k\Omega$, $R_0 = 50\ k\Omega$ and $\beta = -\frac{1}{15}$. **(04 Marks)**

6 a. Enumerate the types of power amplifiers along with their efficiency, conduction angle and Q-point. **(05 Marks)**

b. Prove that the maximum efficiency of a class-B power amplifier is 78.5%. **(05 Marks)**

c. Calculate the efficiency of the following circuit shown in Fig. Q6 (c), for an input current swing of 10 mA. **(05 Marks)**

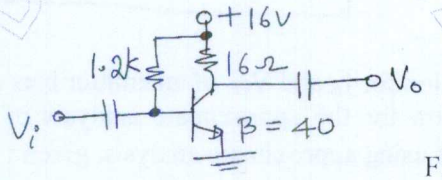

Fig. Q6 (c)

d. Along with the circuit diagram, explain the working of Class-C amplifier. **(05 Marks)**

7 a. Along with the circuit diagram, explain the working of a BJT phase-shift oscillator. **(06 Marks)**

b. Design a Wien-bridge oscillator for $f_0 = 6$ kHz, making suitable assumptions. **(06 Marks)**

c. Along with proper diagrams, explain the series resonant and parallel resonant crystal oscillators using BJT. **(08 Marks)**

8 a. Explain the operation of JFET amplifier using fixed bias. Draw the JFET small signal model, and derive the expressions for Z_i, Z_o and A_V. **(10 Marks)**

b. With necessary circit diagram, obtain the expressions for Z_i, Z_o and A_V for an E-MOSFET voltage-divider configuration. **(10 Marks)**

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